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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,137	08/27/2004	Andrew Crosland	015114-053510US	5136

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,137	CROSLAND ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/1/04, 8/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is with regards to Application No. 10/711,137, filed 27 August 2004. This Application is a divisional of U.S. Patent Application No. 09/880,734, filed 12 June 2001. Claims 1 – 28 are pending in this Application.

Drawings

2. The drawings are objected to because of the reasons indicated in the attached Notice of Draftsperson's Patent Drawing Review (Form PTO-948). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 27 is objected to because of the following issue:

- There is no antecedent basis for "the external source".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,615,167 B1 to Devins et al. (hereinafter, "Devins") in view of U.S. Patent No. 6,096,091 to Hartmann.

6. **Referring to claim 4**, Devins discloses a method comprising designing an embedded processor stripe (i.e., processor core - see Figs. 1 and 3, block 112), contained in an SoC (system-on-chip) integrated circuit (see Abstract). The circuit also includes a watchdog timer circuit (see col. 5, ll. 10 – 15, which cites resetting timers and status registers).

Although Devins teaches SoC integrated circuits and the like (see Devins – col. 1, ll. 29 – 43), he does not specifically teach using a programmable logic integrated circuit in his disclosure.

Hartmann teaches an IC that uses programmable logic with an embedded processor (see Hartmann – col. 2, ll. 35 – 46), but does not teach the inclusion of a watchdog timer.

As stated by Hartmann (col. 1, ll. 39 – 44), using programmable logic brings manufacturing economies of scale to a broad varieties of applications through dynamically reconfigurable logic networks for flexible pipeline processing in an SoC. It would therefore be obvious to a person of ordinary skill in the art at the time of the invention to modify the teachings of Devins with the teachings of Hartmann in order to incorporate an embedded processor core, and a watchdog timer, into a programmable logic circuit.

7. **As for claim 5**, see Hartmann – Fig. 2, blocks 110A, 150 and 160, which show the signal lines of the embedded processor stripe (block 150) coupled to the signal lines of the programmable logic portion (blocks 110A and 160), as claimed.

8. **As for claim 6**, see Devins – Fig. 3, block 112, which shows the embedded processor positioned at the edge of the circuit.

9. **Claims 1, 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devins in view of Hartmann, and further in view of U.S. Patent No. 5,604,680 to Bamji et al. (hereinafter, "Bamji").**

10. **Regarding claim 1**: as indicated in item 5 above, Devins and Hartmann collectively disclose a method of designing a programmable logic IC that includes the layout of an embedded processor stripe and a watchdog timer circuit.

But neither Devins nor Hartmann disclose the claimed limitation of stretching the first layout of a programmable logic IC using an edge of the first layout so the first layout has a stretched section, and incorporating the second layout of an embedded processor stripe that also includes a watchdog timer circuit, and coupling the signal lines of the first layout to the signal lines of the second layout.

However, Bamji provides a method and system for symbolically representing a circuit layout using only topological and connectivity information (Bamji – col. 3, ll. 48 – 50) that also includes stretching and abutting blocks (see Bamji – Figs. 5A, 5C; col. 9, line 61 – col. 10, line 10).

As stated by Bamji (col. 12, ll. 4 – 15), the ability to stretch and abut cells and blocks provides greater flexibility in the layout of complex IC circuits, such as SoC, etc. It would therefore be obvious to a person of ordinary skill in the art at the time the invention was made to be able to modify the teachings of Devins and Hartmann, with the teachings of Bamji in order to provide a method of designing a programmable logic IC by stretching an edge of a first design that contains a

programmable logic circuit, and incorporating a second layout that includes an embedded processor with a watchdog timer.

11. **As for claim 2**, see Hartmann – col. 1, ll. 24 – 44, which disclose the fabrication of the programmable logic device with an embedded processor, as claimed.

12. **As for claim 3,** see item (9) above, which teaches the claimed elements of a programmable logic IC designed according to the method of claim 1.

13. **Claims 7 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devins in view of Hartmann, and further in view of U.S. Patent No. 5,478,618 to Van de Steeg et al. (hereinafter, "Steeg").**

14. **Referring to claim 7**, Devins and Hartmann collectively teach a programmable logic IC comprising an embedded processor portion, and a programmable logic portion, wherein the embedded processor portion includes a watchdog timer circuit (see item (5) above).

However, neither Devins nor Hartmann disclose the additional claimed limitations of having an external configuration source IC, coupled to the programmable logic IC, storing configuration information for the programmable logic IC, wherein when the watchdog timer circuit asserts a triggered signal output due to not reloading the watchdog timer circuit within a timeout period, configuration data is loaded from the external configuration source into the programmable logic IC.

But Steeg teaches an external configuration source IC (a PROM) coupled to the programmable logic IC (see Fig. 28; Abstract; Abstract; col. 3, ll. 30 – 35), storing configuration information for the programmable logic IC (see again col. 3, ll. 32 – 33), wherein when the watchdog timer circuit asserts a triggered signal output due to not reloading the watchdog timer circuit within a timeout period (see col. 3, ll. 34 – 53; col. 8, ll. 49 – 55), configuration data is loaded from the external configuration source into the programmable logic IC (see again col. 3, ll. 28 – 50).

As stated by Steeg, it is advantageous to provide an I/O module with integrated circuitry that is loaded with configuration data across an isolation interface (see Steeg - col. 1, ll. 54 – 56) so that it can be applied in a programmable controller I/O module for controlling motion and for communicating I/O data with a controller processor through a backplane (see Steeg - col. 2, ll. 12 – 15).

It would therefore be obvious to a person of ordinary skill in the art at the time of the invention to modify the teachings of Devins and Hartmann, with the teachings of Steeg, in order achieve a circuit comprising a programmable logic IC with an embedded processor and a watchdog timer that is capable of being configured using an external configuration source IC, and based on a triggered signal output asserted by the watchdog timer circuit.

15. **As per claim 8**, see again Steeg - col. 3, ll. 28 – 41, which shows that the external configuration source is a PROM (i.e., a nonvolatile memory).

16. **As to claim 9**, see Steeg - col. 3, ll. 28 – 53, col. 6, ll. 15 – 39, col. 8, ll. 52 – 56, Table 1, Ref. 60, which disclose the claimed elements pertaining to loading and reloading a reload register of the watchdog timer with one or more "magic" values

17. **As for claims 10 and 11**, see Steeg - Fig. 3, blocks 48 and 44; col. 3, ll. 60 – 62, col. 5, ll. 1 – 15, which disclose using volatile (static) RAM's.

18. **As for claim 12**, see again Steeg - Figs. 2 and 3; col. 3, ll. 28 – 53, which teach configuration data from an external source is used to configure the embedded processor portion as well as the programmable logic portion of the IC as claimed.

19. **As to claim 13**, see Steeg - col. 2, ll. 6 – 9, which disclose the serial transfer of the configuration data, as claimed.

20. **Pursuant to claims 14 and 15**, see Steeg - col. 8, ll. 49 – 59, which teach the claimed limitations of not reloading the watchdog circuit due to a software failure (claim 14), or due to a power supply problem (claim 15).

21. **Claims 16 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devins in view of Hartmann, and further in view of U.S. Patent No. 4,796,211 to Yokouchi et al. (hereinafter, "Yokouchi").**

22. **Referring to claim 16**, Devins and Hartmann collectively teach a programmable logic IC comprising an embedded processor portion, and a programmable logic portion (it is well known in the art that programmable logic arrays are usually arranged in rows

and columns), wherein the embedded processor portion includes a watchdog timer circuit (see item (5) above).

But neither Devins nor Hartmann teach the claimed limitation of the watchdog timer being triggered if a count register of the timer is permitted to count to a final value before the count register is reloaded.

Yokouchi discloses a watchdog timer with a reset detection circuit (see Fig. 1) that indeed includes the timer being triggered if the count register is permitted to count to a final value before the count register is reloaded (in this case the final value is 16 ms – see Yokouchi, col. 1, ll. 36 – 47).

As stated by Yokouchi (col. 1, ll. 63 – 65), it is important to provide a watchdog timer that solves the problem of detecting program runaway. It would therefore be obvious to a person of ordinary skill in the art at the time of the invention to modify the teachings of Devins and Hartmann with the teachings of Yokouchi in order to obtain a programmable logic IC with an embedded processor and a watchdog timer circuit which can be triggered if a count register of the watchdog circuit is permitted to count to a final value.

23. **As per claim 17**, see Yokouchi – col. 1, ll. 48 – 54, which disclose avoiding the triggering of the watchdog circuit, if the watchdog circuit is loaded within a fixed time (i.e., before a timeout period) by means of a magic signal (i.e., carry signal), as claimed.

24. **As per claim 18**, see Yokouchi – col. 1, ll. 42 – 47, which disclose the claimed limitation pertaining to the timeout period being the time it takes for the watchdog timer circuit to count from an initial value ("0") to the final value "16 ms").

25. **Pursuant to claims 19 and 20**, see Hartmann – col. 5, ll. 1 – 8, which cite the inclusion of volatile (RAM) memory cells foe configuring the programmable logic array, as claimed.

26. **As for claim 21**, see Yokouchi – Figs. 1, 2; col. 3, ll. 1 – 36, which teach the claimed elements pertaining to a reload register, and a control register.

27. **As per claim 22**, using a look-up table circuit in programmable logic ICs is inherent, since it speeds up the configuration of such circuits.

28. **As per claim 23**, see Yokouchi – col. 1, ll. 36 – 60, which teach the claimed limitations pertaining the reset circuit of the programmable logic IC.

29. **As for claims 24 and 26**, see Hartmann – Fig. 2, which shows the embedded processor and the embedded processor memory block coupled together by a bus, as claimed.

30. **As per claim 25**, see Yokouchi – Fig. 2, which shows the watchdog timer circuit coupled to a bus.

31. **As for claim 27**, see Hartmann – col. 5, ll. 1 – 8, which teach the types of external source memories that can be used to configure the circuit.

32. **As to claim 28**, see Hartmann – Fig. 2; col. 5, line 44 – col. 6, line 6, which disclose a serial stream of bits transferred to the programmable logic IC, as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Magid Y Dimyan
Examiner
Art Unit 2825

myd
30 May 2007

MYD

JACK CHIANG
SUPERVISORY PATENT EXAMINER